

I claim:

1. A frequency synchronizer system, comprising:

a processor for executing a sequence of operations, where said operations include:

a) initializing an estimated frequency correction factor;

b) determining a corrected frequency offset value from a first product of a sample signal and said estimated frequency correction factor;

c) filtering a first sample of said corrected frequency offset value to obtain a filtered corrected frequency offset value;

d) imparting a delay to a second sample of said corrected frequency offset value to obtain a delayed corrected frequency offset value;

e) determining a conjugate product value from a second product of said filtered corrected frequency offset value and a conjugate of said filtered corrected frequency offset value;

f) determining a delay conjugate value from a third product of said delayed corrected frequency offset value and said conjugate product value;

g) determining an error signal from said delay conjugate value;

h) determining a frequency offset value from said error signal; and

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26 i) determining an updated value of said estimated frequency correction factor from said
27 frequency offset value

1 2. The frequency synchronizer system of claim 1 wherein said operations (b) through (i) are
2 repeated an integral number of times.

1 3. The frequency synchronizer system of claim 1 further including a digital receiver for
2 providing an estimate of data encoded in a continuous-phase modulation signal in response to
3 receiving said corrected frequency offset value.

1 4. The frequency synchronizer system of claim 1 further including an anti-aliasing filter for
2 transforming said continuous-phase modulation signal into a filtered signal.

1 5. The frequency synchronizer system of claim 4 further including a sampler for transforming
2 said filtered signal into a sequence of discrete time based samples.

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